

# Contents

## IPFA 2011 Best Paper

### **Electrical Failure and Damage Analysis of Multi-Layer Metal Films on Flexible Substrate during Cyclic Bending Deformation .....**1

*Byoung-Joon Kim<sup>1</sup>, Hae-A-Seul Shin<sup>1</sup>, In-Suk Choi<sup>2</sup>, and Young-Chang Joo<sup>1</sup>*

*1) Seoul National University, Seoul, Korea*

*2) Korea Institute of Science and Technology, Seoul, Korea*

## Session 1: Emerging FA Techniques and Concepts

### **A Position-Sensitive, Single-Photon Detector with Enhanced NIR Response.....5**

*Franco Stellari<sup>1</sup>, Peilin Song<sup>1</sup>, Alan J. Weger<sup>1</sup>, Tomonori Nakamura<sup>2</sup>, Stanley Kim<sup>2</sup>, and Robert Roche<sup>2</sup>*

*1) IBM T.J. Watson Research Center, Yorktown Heights, NY, USA*

*2) Hamamatsu Photonics, Japan & USA*

### **Advanced Scan Chain Failure Analysis Using Laser Modulation Mapping and Continuous Wave Probing .....**12

*Steven Kasapi, William Lo, Joy Liao, Bruce Cory, and Howard Marks,  
NVIDIA, Santa Clara, CA, USA*

### **Thermal Frequency Imaging: A New Application of Laser Voltage Imaging Applied on 40nm Technology .....**18

*Guillaume Celi<sup>1</sup>, Sylvain Dudit<sup>1</sup>, Thierry Parrassin<sup>1</sup>, Philippe Perdu<sup>2</sup>, Antoine Reverdy<sup>3</sup>,  
Dean Lewis<sup>4</sup>, and Michel Vallet<sup>1</sup>*

*1) STMicroelectronics, Crolles, France*

*2) CNES Laboratory, Toulouse, France*

*3) SECTOR Technologies, Gières, France*

*4) Univ. Bordeaux, Talence, France*

### **Local Lattice Strain Measurement Using Geometric Phase Analysis of Dark Field Images from Scanning Transmission Electron Microscopy .....**24

*Jayhoon Chung<sup>1</sup>, Guoda Lian<sup>1</sup>, and Lew Rabenberg<sup>2</sup>*

*1) Texas Instruments, Dallas, TX, USA*

*2) University of Texas, Austin, TX, USA*

### **Correcting for Spherical Aberrations in Solid Immersion Microscopy Using a Deformable Mirror .....**26

*Y. Lu, E. Ramsay, C. Stockbridge, F.H. Koklu, A. Yurt, J. Mertz, T.G. Bifano,  
M.S. Ünlü and B.B. Goldberg, Boston University, Boston, MA, USA*

## Session 2: Circuit Edit

<b>The Challenges of Backside Focused Ion Beam (FIB) Editing in the Presence of Deep Trench Decoupling Capacitors .....</b>	<b>31</b>
<i>Steven B. Herschbein, Carmelo F. Scrudato George K. Worth, and Edward S. Hermann, IBM Systems &amp; Technology, Hopewell Junction, NY, USA</i>	
<b>State of the Art Substrate Manipulation as a Tool for Enhancing Product Performance.....</b>	<b>35</b>
<i>Michael A. Gonzales and Jose Cabanillas, Qualcomm, San Diego, CA, USA</i>	
<b>Neon Ion Microscope Nanomachining Considerations .....</b>	<b>40</b>
<i>Shida Tan<sup>1</sup>, Richard H. Livengood<sup>1</sup>, Roy Hallstein<sup>1</sup>, Darryl Shima<sup>1</sup>, Yuval Greenzweig<sup>1</sup>, John Notte<sup>2</sup>, and Shawn McVey<sup>2</sup></i>	
1) Intel Corporation, Santa Clara, CA, USA	
2) Carl Zeiss SMT, Peabody, MA, USA	
<b>Instant Solid Immersion Lens Creation in Silicon with a Focused Ion Beam – Comparing Refractive and Diffractive Methods .....</b>	<b>46</b>
<i>P. Scholz<sup>1</sup>, U. Kerst<sup>1</sup>, C. Boit<sup>1</sup>, T. Kujawa<sup>2</sup>, and T. Lundquist<sup>2</sup></i>	
1) Berlin University of Technology, Berlin, Germany	
2) DCG Systems, Fremont, CA, USA	
<b>Circuit Edit and Optical Probe Development and Validation for Next Generation Process Nodes .....</b>	<b>54</b>
<i>John A. Giacobbe<sup>1</sup>, Patrick Pardy<sup>2</sup>, Charles A. Peterson<sup>2</sup>, David Shykind<sup>2</sup>, and Scot E. Zickef<sup>2</sup></i>	
1) Intel Corporation, Folsom, CA, USA	
2) Intel Corporation, Hillsboro, OR, USA	

## Session 3: Packaging and Assembly Level FA I

<b>3DIC Fault Isolation Using the OBIRCH Approach .....</b>	<b>60</b>
<i>Ming-Sung Hsu, Yian-Liang Kuo, Yu-Ting Lin, Ru-Ying Huang, Min-Feng Ku, and Chih-Horng Chang, Taiwan Semiconductor Manufacturing Company, Ltd., Hsin-Chu, Taiwan</i>	
<b>Improving Wire Sweep Performance by Measuring Degree of Cure of Epoxy Mold Compounds .....</b>	<b>64</b>
<i>Sheila Liza B. Dal, ON Semiconductor Philippines Inc., Cavite, Philippines</i>	
<b>Use of Lock-In Thermography for Non-Destructive 3D Defect Localization on System in Package and Stacked-Die Technology .....</b>	<b>68</b>
<i>Rudolf Schlangen<sup>1</sup>, Shinobu Motegi<sup>1</sup>, Toshi Nagatomo<sup>1</sup>, Christian Schmidt<sup>2</sup>, Frank Altmann<sup>2</sup>, Hiroaki Murakami<sup>3</sup>, Stewart Hollingshead<sup>4</sup>, and John West<sup>4</sup></i>	
1) DCG Systems, Fremont, CA, USA	
2) Fraunhofer Institute for Mechanics of Materials, Halle, Germany	
3) Toshiba, Yokohama, Japan	
4) Texas Instruments, TX, USA	

<b>Quantitative Phase Shift Analysis for 3D Defect Localization Using Lock-in Thermography .....</b>	<b>74</b>
<i>Christian Schmidt and Frank Altmann, Fraunhofer Institute for Mechanics of Materials IWM, Halle, Germany</i>	
<b>Failure Analysis of Flip Chip C4 Package Using Focused Ion Beam Milling Technique .....</b>	<b>81</b>
<i>Lihong Cao, Loc Tran, and Wallace Donna, Advanced Micro Devices, Inc., Austin, TX, USA</i>	
 <b>Session 4: Test and Diagnostics</b>	
<b>Layout-Aware Diagnosis Leads to Efficient and Effective Physical Failure Analysis .....</b>	<b>86</b>
<i>Manish Sharma<sup>1</sup>, Sergej Schwarz<sup>1</sup>, Juergen Schmerberg<sup>1</sup>, Kathy Yang<sup>1</sup>, Ting-Pu Tai<sup>1</sup>, Yuan-Shih Chen<sup>2</sup>, Cheng-Yiing Chuang<sup>2</sup>, Feng-Ming Kuo<sup>2</sup>, Mike Brennan<sup>3</sup>, James Yeh<sup>3</sup>, and Alan Ma<sup>3</sup></i>	
1) Mentor Graphics Corporation, Wilsonville OR, USA	
2) Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, ROC	
3) AMD, Sunnyvale CA, USA	
<b>Device Selection for Failure Analysis of Chain Fails Using Diagnosis Driven Yield Analysis .....</b>	<b>91</b>
<i>Chris Schuermyer<sup>1</sup>, Brady Benware<sup>1</sup>, Graham Rhodes<sup>2</sup>, Davide Appello<sup>3</sup>, Vincenzo Tancorre<sup>4</sup>, Olivia Riewer<sup>5</sup></i>	
1) Mentor Graphics Corp., Wilsonville, Oregon, USA	
2) Mentor Graphics Corp., Grenoble, France	
3) STMicroelectronics, Agrate Brianza, Italy	
4) STMicroelectronics, Rousset, France	
5) STMicroelectronics, Grenoble, France	
<b>Debugging an Invisible Flaky Scan Chain Defect .....</b>	<b>98</b>
<i>Rahul Shukla<sup>1</sup>, Richard Billings<sup>2</sup>, Anurag Bakhshi<sup>2</sup>, John Schulze<sup>2</sup>, Atchayuth Gorti<sup>2</sup>, and Nagesh Tamarapalli<sup>1</sup></i>	
1) AMD India Private Limited, Shivajinagar, Bangalore India	
2) Advanced Micro Devices Inc., Austin, TX, USA	
<b>Diagnose Compound Hold Time Faults Caused by Spot Delay Defects at Clock Tree .....</b>	<b>103</b>
<i>Yu Huang<sup>1</sup>, Wu-Tung Cheng<sup>1</sup>, Ting-Pu Tai<sup>1</sup>, Liyang Lai<sup>1</sup>, Ruifeng Guo<sup>1</sup>, Feng-Ming Kuo<sup>2</sup>, and Yuan-Shih Chen<sup>2</sup></i>	
1) Mentor Graphics Corporation, Wilsonville, OR, USA	
2) Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C.	

## **Session 5: Defect Characterization and Metrology**

<b>A Comprehensive Analysis Methodology for Gate Oxide Integrity Failure Using Combined FA Techniques .....</b>	<b>112</b>
<i>Hua Younan, Nistala Ramesh Rao, Chen Shuting, Zhu Lei, Chia Chin Ning, Zhang Jianming, Huang Yanhua, and Neo Soh Ping, GLOBALFOUNDRIES Singapore, Singapore</i>	

<b>Al Bondpads, Halogens, and an ESCA-Based Search for the Invisible Cause of Poor Throughput at Wafer Probe .....</b>	<b>118</b>
<i>David W. Niles and Ronald W. Kee, Avago Technologies, Fort Collins, CO, USA</i>	
<b>Whisker Formation in Copper Electroplating .....</b>	<b>127</b>
<i>Theresa Han, Eunin Cho, Jinwoo Heo, and Seoung Jae Lee, Samsung Electro-Mechanics. Co., Ltd., Chungnam-Do, Republic of Korea</i>	
<b>Comprehensive Nano-Structural Approach of SSRM Nanocontact on Silicon through TEM-STEM Study .....</b>	<b>132</b>
<i>B. Domengès<sup>1</sup>, T. Delaroque<sup>2</sup>, K. Danilo<sup>2</sup>, and A. Colde<sup>2</sup> 1) LAMIPS, CRISMAT – NXP Semiconductors, Caen, France 2) Presto-Engineering Europe, Caen, France</i>	
<b>Highly Automated Transmission Electron Microscopy Tomography for Defect Understanding .....</b>	<b>137</b>
<i>James J. Demarest and Hong-Ying Zhai, IBM, Albany, NY, USA</i>	

<b>Transmission Electron Microscopy Characterization of FinFET – Understanding the 3D Structure by 2D Imaging Technique .....</b>	<b>141</b>
<i>Yu Zhu and Jemima Gonsalves, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA</i>	

## Session 6: Photon Based Fault Isolation Techniques

<b>A Comparison of Lock-in Thermography and Magnetic Current Imaging for Localizing Buried Short-Circuits .....</b>	<b>146</b>
<i>David P. Vallett, IBM Systems &amp; Technology Group, Essex Junction, VT, USA</i>	

<b>Scan Chain Debug Using Dynamic Lock-In Thermography .....</b>	<b>153</b>
<i>L. Forli<sup>1</sup>, B. Picart<sup>1</sup>, A. Reverdy<sup>2</sup>, and R. Schlangen<sup>3</sup> 1) LFoundry, Rousset, France 2) Sector Technologies, Gières, France 3) DCG Systems, Fremont, CA, USA</i>	

<b>Practical Implementation of Soft Defect Localization (SDL) in Mixed Signal and Analog ICs .....</b>	<b>158</b>
<i>Eric Barbier, Gretchen Crow, Win Thandar Swe, and Mark C. Phillips, ON Semiconductor, Phoenix, AZ, USA</i>	

<b>Photon Emission Spectra through Silicon of Various Thicknesses .....</b>	<b>164</b>
<i>Arkadiusz Glowacki<sup>1</sup>, Carlo Pagano<sup>1</sup>, Christian Boit<sup>1</sup>, Yoshiyuki Yokoyama<sup>2</sup>, Arkadiusz Jankowski<sup>3</sup>, and Philippe Perdu<sup>4</sup>, 1) Berlin University of Technology, Berlin, Germany 2) Hamamatsu Photonics Germany, Herrsching, Germany 3) Technical University of Łódź, Łódź, Poland 4) French Space Agency, CNES, Toulouse, France</i>	

<b>Characterization of MOS Transistors Using Dynamic Backside Reflectance Modulation Technique .....</b>	<b>170</b>
<i>J.K.J. Teo<sup>1</sup>, C.M. Chua<sup>2</sup>, L.S. Koh<sup>2</sup>, J.C.H. Phang<sup>1,2</sup></i>	
1) National University of Singapore, Singapore	
2) SEMICAPS Pte. Ltd., Singapore	

## **Session 7: FA Process and Case Studies I**

<b>Effective Fault Isolation Using Memory BIST and Logic BIST Diagnostic Techniques .....</b>	<b>176</b>
<i>Rakesh Kinger<sup>1</sup>, Chuck Tong<sup>1</sup>, Ayyaz Chaudhry<sup>1</sup>, Vijay Chowdhury<sup>2</sup>, Wenzhen Sun<sup>2</sup>, Hongqi Deng<sup>2</sup>, and Steve Smith<sup>2</sup></i>	
1) Broadcom Corporation, San Jose, CA, USA	
2) Evans Analytical Group, Sunnyvale, CA, USA	

<b>DRAM Static Refresh Weak Cell Characterization and Structure Analysis .....</b>	<b>182</b>
<i>Sung Ho Lee, Yong Ho Yoo, Tae Jung Park, Jin Choi, Ju Hyeon Ahn, Seok Sik Kim, Chang-Jin Kang, Seok Woo Nam, Joo Young Lee, and Gyo Young Jin, Semiconductor R&amp;D Center Samsung Electronics Co., Ltd., Gyeonggi-Do, Korea</i>	

<b>A Systematic Failure Analysis to Reveal the Mystery of Lower N-Well Resistance .....</b>	<b>185</b>
<i>David Zhu, Soh Ping Neo, Alfred Quah, Ghim Boon Ang, Lei Zhu, Yanhua Huang, Hong Tak Koo, Moi Kian Yau, Ma Hninhnin, and Nagalingam Dayanand, GLOBALFOUNDRIES, Singapore Pte. Ltd., Singapore</i>	

## **Session 8: Finding the Invisible Defect**

<b>From the Store Shelf to Device-Level Atom Probe Analysis: An Exercise in Feasibility .....</b>	<b>189</b>
<i>D.J. Larson<sup>1</sup>, D. Lawrence<sup>1</sup>, D. Olson<sup>1</sup>, T.J. Prosa<sup>1</sup>, R.M. Ulfig<sup>1</sup>, D.A. Reinhard<sup>1</sup>, P.H. Clifton<sup>1</sup>, T.F. Kelly<sup>1</sup>, and W. Lefebvre<sup>2</sup></i>	
1) Cameca Instruments Inc., Madison, WI, USA	
2) Université de Rouen, Saint Etienne du Rouvray, France	

<b>Non-Visible Defect Analysis of OTP Device .....</b>	<b>198</b>
<i>C.Q. Chen, G.B. Ang, Z.X. Xing, Y.N. Hua, Z.Q. Mo, Rao Ramesh, and Y. Li, GLOBALFOUNDRIES Singapore, Singapore</i>	

<b>Addressing Stress-Memorization-Technology (SMT) Induced Defects .....</b>	<b>202</b>
<i>Terence Kane, Yun Yu Wang, Michael Tenney, Richard Oldrey, Manuel Villalobos, John Sylvestri, and Genadi Tverskoy, IBM Systems and Technology Group, Hopewell Junction, NY, USA</i>	

<b>Flash Single Bit Cycling Fail Due to Charge Accumulation from Incorrect Lateral Drain Junction Formation .....</b>	<b>207</b>
<i>Keith Harber, Sam Subramanian, Tony Chrastecky, Khiem Ly, and Fuchen Mu, Freescale Semiconductor, Inc., Austin, TX, USA</i>	

<b>Identification of Extension Implant Defect in Sub-Micron CMOS ICs – Analysis Technique, Model, and Solution .....</b>	<b>212</b>
<i>Yuk L. Tsang<sup>1</sup>, Giri Nallapati<sup>2</sup>, Ron Skarupa<sup>1</sup>, and Brian Anthony<sup>1</sup></i>	
1) Freescale Semiconductor Inc., Austin, TX, USA	
2) Qualcomm, San Diego, CA, USA	
<b>A Sample Preparation Technique to Localize Gate Oxide Defects in Memory Arrays Using Conducting Atomic Force Microscopy .....</b>	<b>218</b>
<i>Lakshminarayanan Lakshmanan<sup>1</sup>, Lowell Herlinger<sup>1</sup>, and Kathryn Miller<sup>2</sup></i>	
1) Advanced Micro Devices, Inc., Austin TX, USA	
2) Samsung Electronics, Austin TX, USA	

## **Session 9: MEMS, Discretes and Optoelectronics Device FA**

<b>Failure Analysis on Power Trench MOSFET Devices with Copper Wire Bonds .....</b>	<b>223</b>
<i>Huixian Wu, Arthur Chiang, David Le, and Win Pratchayakun, Vishay Siliconix, Santa Clara, CA, USA</i>	
<b>Infrared Thermography Developments for III-V Transistors and MMICs .....</b>	<b>230</b>
<i>Dominique Carisetti<sup>1</sup>, Mohsine Bouya<sup>1</sup>, Odile Bezencenet<sup>1</sup>, Bernard Servet<sup>1</sup>, Jean-Claude Clément<sup>1</sup>, Benoit Lambert<sup>2</sup>, Laurent Caille<sup>2</sup>, Nathalie Malbert<sup>3</sup>, and Nathalie Labat<sup>3</sup></i>	
1) Thales Research and Technology, Palaiseau, France	
2) United Monolithic Semiconductors, Orsay Cedex, France	
3) University Bordeaux, Talence, France	

## **Session 10: Counterfeit Microelectronics Detection and Mitigation**

<b>Detection of a Counterfeit OTA Device and Certification of a Replacement Source .....</b>	<b>234</b>
<i>Yong Hong, Harman International Automotive Division, Farmington Hills, MI, USA</i>	
<b>DNA to Safeguard Electrical Components and Protect Against Counterfeiting and Diversion .....</b>	<b>238</b>
<i>James A. Hayward, and Janice Meraglia, Applied DNA Sciences, Stony Brook, NY, USA</i>	

## **Session 11: Sample Preparation and Device Deprocessing I**

<b>Backside De-Processing of Integrated Circuits 40 nm and Below .....</b>	<b>242</b>
<i>Yuanjing Li, Steven Scott, and Howard Lee Marks, NVIDIA Corporation, Santa Clara, CA, USA</i>	

<b>New Method for Decapsulation of Copper Wire Devices Using LASER and Subambient Temperature Chemical Etch .....</b>	<b>248</b>
Matthew J. Lefevre <sup>1</sup> , Frédéric Beauquis <sup>1</sup> , Michael Obein <sup>1</sup> , Pascal Gounet <sup>2</sup> , and Sandrine Barberan <sup>2</sup>	
1) Digit Concept, Secqueville en Bessin, France	
2) ST Ericsson, Grenoble, France	

<b>New Front Side Access Approach for Low-k Dielectric/Cu Technologies in Plastic Package .....</b>	<b>256</b>
Amandine Aubert <sup>1</sup> , Lionel Dantas de Moraes <sup>1</sup> , Stéphanie Pétrémont <sup>1</sup> , Nathalie Labat <sup>2</sup> , and Hélène Frémont <sup>2</sup>	
1) STMicroelectronics, Tours, France	
2) University Bordeaux, Bordeaux, France	

<b>A Novel Low Cost Technique to Perform Concurrent Topside and Backside Analysis of a Bare Die .....</b>	<b>262</b>
Raj Kabadi and Win Thandar Swe, ON Semiconductor, Phoenix, AZ, USA	

## **Session 12: Nanoprobing and Electrical Characterization I**

<b>Electrical Signature Verification and Fault Localization in High-Density DRAM Device Using Atomic Force Probe .....</b>	<b>269</b>
Wei-Chih Wang, San-Lin Liew, Hua-Sheng Chen, Kuang-Liang Chen, and Jian-Shing Luo, Inotera Memories, Inc., Taoyuan, Taiwan, Republic of China	

<b>Advanced Backside Defect Isolation Techniques Using Electron Beam Absorbed Current to Locate Metal Defectivity on Bulk and SOI Technology .....</b>	<b>275</b>
K. Erington, K. Dickson, G. Lange, J.Z. Garcia, J. Ybarra, and N. Wetterling, Freescale Semiconductor, Inc., Austin, TX	

<b>A Study of a Characteristics Variability Evaluation in an Actual LSI Circuit with Nanoprobing Technique .....</b>	<b>287</b>
Munetoshi Fukui <sup>1,2</sup> , Yasuhiko Nara <sup>1</sup> , Takaaki Tsunomura <sup>2</sup> , Akio Nishida <sup>2</sup> , and Junichi Fuse <sup>3</sup>	
1) Hitachi High-Technologies, Hitachinaka, Ibaraki, Japan	
2) MIRAI-Selete, Tsukuba, Ibaraki Japan	
3) Hitachi High-Tech Manufacturing & Service, Hitachinaka, Ibaraki, Japan	

<b>Fault Isolation of Dense High Rc Array by Using Conductive Atomic Force Microscopy .....</b>	<b>293</b>
Wei-Shan Hu, Hui-Wen Yang, and Yung-Sheng Huang, Taiwan Semiconductor Manufacturing Company, Ltd., Hsin-Chu, Taiwan, R.O.C.	

## **Session 13: Sample Preparation and Device Deprocessing II**

<b>Development of a Protective Coating for Application of Ion Cross-Section Polishing on Thermal Inkjet Printhead Heater Chips .....</b>	<b>296</b>
Q. Zhang and X.M. Wu, Lexmark International, Inc. Lexington, KY, USA	

<b>Impacts of Sample Preparation Methodology on TEM Failure Analysis of Advanced Semiconductor Devices .....</b>	<b>301</b>
<i>Yongkai Zhou, Jie Zhu, Han Wei Teo, ACT Quah, Lei Zhu, Anyan Du, and Younan Hua, GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore</i>	

<b>TEM Sample Preparation by Single-Sided Low-Energy Ion Beam Etching .....</b>	<b>305</b>
<i>Liew Kaeng Nan and Lee Meng Lung, United Microelectronics Corporation (Singapore Branch), Ltd., Singapore</i>	

<b>Multiple-Post In-Situ Lift-Out Grids Preparation Using a Dicing Saw .....</b>	<b>308</b>
<i>Jian-Shing Luo, Hsiu-Ting Lee, San-Lin Liew, Ching-Shan Sung, and Yi-Jing Wu, Inotera Memories, Inc. Taoyuan, Taiwan, Republic of China</i>	

## **Session 14: Nanoprobing and Electrical Characterization II**

<b>Scanning Capacitance Microscopy: A Valuable Tool to Diagnose Current Paths in 3D-Capacitors Process.....</b>	<b>316</b>
<i>Thomas Delaroque<sup>1</sup>, Karine Danilo<sup>1</sup>, Frédéric Voiron<sup>2</sup>, Catherine Bunel<sup>2</sup>, Bernadette Domengès<sup>3</sup>, Marc Laflutte<sup>4</sup>, and Renzo Dalmolin<sup>4</sup> 1) Presto-Engineering, Caen, France 2) Ipdia, Caen, France 3) LAMIPS, CRISMAT, Caen, France 4) Sorin, Clamart, France</i>	

<b>Nano Probe Analysis of Device Characteristics Affected by Ring Type Crystalline Defect .....</b>	<b>322</b>
<i>Jong Hak Lee, Yu Jun Lee, Jung Sam Kim, Seo Kyung Jeong, Min Su Kim, Seok Hoon Oh, Kyoung Wook Jung, Soo Yong Son, and Chang Reol Kim, Hynix Semiconductor Inc., Ichon-si, Kyoungki-do, Korea</i>	

<b>Electroless Cobalt Plating on Copper Structures for Nano-Probing .....</b>	<b>327</b>
<i>Wen-Hsien Chuang, Ting Zhong, and Baohua Niu, Intel Corporation, Hillsboro, OR, USA</i>	

## **Session 15: Alternative Energy**

<b>Can Illuminated IV-Characteristics of Micro-Regions in Solar Cells be Measured by Laser-Induced Stimulation? .....</b>	<b>330</b>
<i>M. Boostandoost, A. Glowacki, O. Bakaeva, U. Kerst, and C. Boit, Berlin University of Technology, Berlin, Germany</i>	

<b>Setup for Locating PV-Cell Defects through <math>I_{sc}</math> Measurements .....</b>	<b>336</b>
<i>Santhosh Shankar, Andreas Bernhardt, Balaji Srinivasan, Sravanthi Enimidisetti, and Martin Versen, University of Applied Sciences Rosenheim, Rosenheim, Germany</i>	

<b>All-Contactless Measurement of Series Resistance Distributions on Solar Cells with Photoluminescence Imaging .....</b>	<b>340</b>
<i>M. Kasemann<sup>1</sup>, L.M. Reindl<sup>1</sup>, B. Michl<sup>2</sup>, W. Warta<sup>2</sup>, A. Schütt<sup>3</sup>, and J. Carstensen<sup>3</sup></i>	
1) <i>Albert-Ludwig Universität, Freiburg, Germany</i>	
2) <i>Fraunhofer Institute for Solar Energy Systems ISE, Freiburg, Germany</i>	
3) <i>University of Kiel, Kiel, Germany</i>	

## **Session 16: FA Process and Case Studies II**

<b>Fast Diagnosis and Failure Mechanism of Phosphorous Contamination in Arsenic-Implanted Silicon .....</b>	<b>345</b>
<i>Lei Zhu, H.W. Teo, K. Ong, Y.H. Huang, R. Koh, P.Y. Chew and Y.N. Hua, GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore</i>	

<b>Failure Analysis Methodology on Unique 68mm Single Ring Pattern Due to Load Lock Burr .....</b>	<b>349</b>
<i>A.C.T Quah, G.B. Ang, C.Q. Chen, David Zhu, M. Gunawardana, J. Indahwan, M.T. Lee , S.P. Neo, and Y. Chen, GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore</i>	

<b>Influence of Laser Radiation on Embedded Non Volatile Memories and Its Application for Descrambling Verification .....</b>	<b>354</b>
<i>I. Österreicher, J. Skuras, and A. Haase, Infineon Technologies Dresden GmbH, Dresden, Germany</i>	

<b>Systematic EFA Approach in Locating Floating Nodes in Analog Mixed Signal Devices .....</b>	<b>359</b>
<i>Sagar Karki, Texas Instruments Inc., Dallas, TX, USA</i>	

<b>Challenges and Benefits of Product-Like SRAM in Technology Development .....</b>	<b>362</b>
<i>Felix Beaudoin<sup>1</sup>, Stephen Lucarini<sup>1</sup>, Fred Towler<sup>1</sup>, Stephen Wu<sup>1</sup>, Zhigang Song<sup>1</sup>, David Albert<sup>1</sup>, Laura Safran<sup>1</sup>, John Sylvestri<sup>1</sup>, Gauri Karve<sup>1</sup>, Xiaojun Yu<sup>1</sup>, Eli Kachir<sup>2</sup>, and Noam Jungmann<sup>2</sup></i>	
1) <i>IBM Systems and Technology, Hopewell Junction, NY, USA</i>	
2) <i>IBM Systems and Technology, Ramat Hahayal, Israel</i>	

## **Session 17: Posters**

<b>Activity Analysis at Low Power Supply on 45nm Technology .....</b>	<b>367</b>
<i>Guillaume Bascoul<sup>1</sup>, Philippe Perdu<sup>1</sup>, Kevin Sanchez<sup>1</sup>, Dean Lewis<sup>2</sup>, Sylvain Dudit<sup>3</sup>, and Guillaume Celi<sup>3</sup></i>	
1) <i>CNES, Toulouse, France</i>	
2) <i>Université de Bordeaux, Talence, France</i>	
3) <i>ST Microelectronics, Crolles, France</i>	

<b>CHIPSCANNER: Reverse Engineering Solution for Microchips at the Nanometer-Scale .....</b>	<b>373</b>
<i>Joseph Klingfus<sup>1</sup>, Kevin Burcham<sup>1</sup>, Martin Rasche<sup>2</sup>, Thomas Borcherf<sup>2</sup>, and Niklas Damnik<sup>2</sup></i>	
1) Raith USA, Inc., Ronkonkoma, NY, USA	
2) Raith GmbH, Dortmund, Germany	
<b>Acoustic Micro Imaging of Large Objects .....</b>	<b>377</b>
<i>Daniel J.D. Sullivan and Jesse A. Guzman, ISE Labs, Fremont, CA, USA</i>	
<b>Design Based Failure Analysis of a Voltage Sensitive Memory Defect .....</b>	<b>382</b>
<i>Andrew Bowsher, Cary A. Gloor, Bruce Griffiths, and Chris McMahon, LSI Corporation, Fort Collins, CO, USA</i>	
<b>Failure Analysis Method of Using Laser Nano Electrostaticfield Probe Sensor (L-NEPS) .....</b>	<b>387</b>
<i>Seigo Ito<sup>1</sup>, Hiroko Sodeyama<sup>1</sup>, Kyoaki Takiguchi<sup>1</sup>, and Toru Matsumoto<sup>2</sup></i>	
1) The University of Tokyo, Tokyo, Japan,	
2) Hamamatsu Photonics K.K., Hamamatsu City, Japan	
<b>Split-Gate Flash Memory Cell Odd/Even Fail Pattern Failure Analysis .....</b>	<b>393</b>
<i>Re-Long Chiu, Jason Higgins, Shu-Lan Ying, Jones Chung, Gang Wang, Xu Liu, and Ty Lim, WaferTech LLC, Camas, WA, USA</i>	
<b>Failure Localization by Using a Novel Backside Passive Voltage Contrast Methodology .....</b>	<b>396</b>
<i>Kuo Hsiung Chen, Chih-Chung Chang, and Jian Chan Lin, United Microelectronics Corporation, Tainan, Taiwan, ROC</i>	
<b>Novel Gox Inspection Methodology in Advanced Silicon Process .....</b>	<b>399</b>
<i>Kuo Yu Wang, Kuo Hsiung Chen, Jian Chang Lin, and W.S. Wu, United Microelectronics Corporation, Ltd., Tainan City, Taiwan, R.O.C.</i>	
<b>A Novel ONO Inspection Methodology for DRAM Deep Trench Structure .....</b>	<b>403</b>
<i>Kuo Hsiung Chen, Chih-Chung Chang, and Jian Chan Lin, United Microelectronics Corporation, Tainan, Taiwan, ROC</i>	
<b>Chromatic Aberration Correction of Silicon Aplanatic Solid Immersion Lens for Photon Emission Microscopy of Integrated Circuits .....</b>	<b>406</b>
<i>A. Yurt, E. Ramsay, F.H. Köklü, M.S. Ünlü and B.B. Goldberg, Boston University, Boston, MA, USA</i>	
<b>Development of an Automated TDR System for Package Failure Analysis .....</b>	<b>410</b>
<i>Christopher C. Basilio<sup>1</sup>, Hieu Trong Nguyen<sup>1</sup>, Arlene Aguinaldo<sup>1</sup>, Jan Paul Arboleda<sup>1</sup>, Richmond Ang<sup>2</sup>, Daniel Ano<sup>2</sup>, Paul Paranao<sup>2</sup>, and Armand Magpantay<sup>2</sup></i>	
1) Vietnam Assembly Test, HCMC, Vietnam	
2) Intel Technology, Trias, Philippines	

<b>Hardness of Rinse Water and Swelling Behavior of Dry Film Photo-Resist .....</b>	<b>414</b>
Song-I. Kim, JinWoo Heo, YunHee Kim, Yeonseop Yu, ChungSik Choi, and JaeSu Yu, Samsung Electro-Mechanics Co., Ltd., Chungnam-Do, Republic of Korea	
<b>A New Failure Analysis Roadmap for Power Semiconductor Modules and Devices .....</b>	<b>419</b>
Peter Jacob <sup>1,2</sup> , Albert Kunz <sup>1</sup> , and Giovanni Nicoletti <sup>1</sup> 1) EMPA Material Science & Technology, Duebendorf, Switzerland 2) RoodMicrotec GmbH, Stuttgart/Noerdlingen, Germany	
<b>A Method of Stress Reduction during Silicon Thinning.....</b>	<b>424</b>
Matthew M. Mulholland <sup>1</sup> and Robert P. Wadell <sup>2</sup> , 1) Intel Corporation, Santa Clara, CA USA 2) Intel Corporation, Folsom, CA USA	
<b>Methodology and Application of Backside Physical Failure Analysis .....</b>	<b>428</b>
Li-Lung Lai <sup>1</sup> , HungLing Chen <sup>1</sup> , and Huimin Gao <sup>2</sup> 1) Semiconductor Manufacturing International Corp., Shanghai, China 2) WuHan Xinxin Semiconductor Manufacturing Corp., WuHan, HuBei, China	
<b>A Study of SRAM Device Soft Failures Caused by Contact Volcano Defects Using Nanoprobing Analysis .....</b>	<b>434</b>
Yu Hsiang Shu, Vincent Huang, and Chia Hsing Chao, United Microelectronics Corporation, Ltd. Taiwan, R.O.C.	
<b>New Failure Analysis Method for Laser Voltage Probing (LVP) Utilizing System Evaluation Board and Software .....</b>	<b>439</b>
Suk Ho Lee, Yun Woo Lee, Moo Jong Hong, Sung Jun Yun, Eun Cheol Lee, and Kyu Shik Hong, Samsung Electronics Co. Ltd., Ki-hung, South Korea	
<b>Evaluation of Electrical Properties of Cell Area on the Semiconductor Devices by FIB Technique .....</b>	<b>443</b>
Jangwon Oh, Jonghyeb Kim, Jonghak Lee, Jongmin Kim, Taesun Back, Won Kim, Hojoung Kim, and Changreol Kim, Hynix Semiconductor Inc., Kyoungki-do, Korea	
<b>Manuscript from 2010 Conference</b>	
<b>The “Perfect Storm” Now Appearing in FA Labs Everywhere .....</b>	<b>446</b>
Gary F. Shade <sup>1</sup> and Bhanu Sood <sup>2</sup> 1) Insight Analytical Labs, Colorado Springs, CO, USA 2) University of Maryland, College Park, MD, USA	
<b>Author Index .....</b>	<b>453</b>