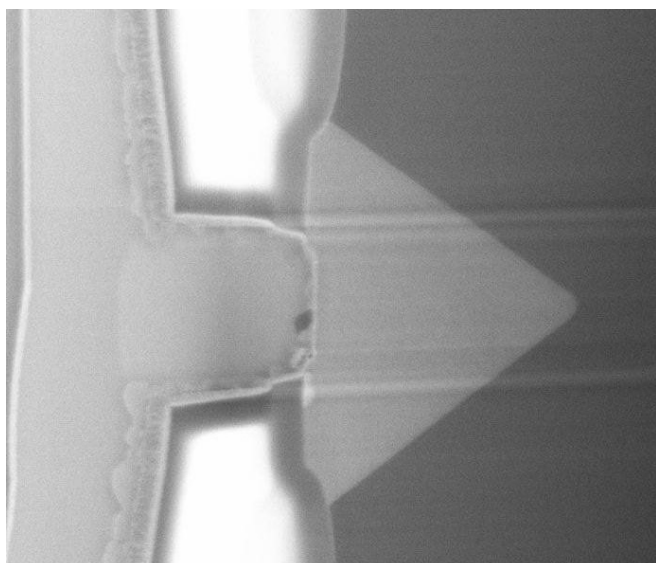


ISTFA™ 2012

Conference Proceedings from the 38th International Symposium for Testing and Failure Analysis

November 11–15, 2012
Phoenix Convention Center
Phoenix, Arizona, USA



The picture shows an FIB cross section through a defective aluminum contact structure. In the silicon-substrate, under the contact, a perfect geometric shaped material interdiffusion (Al-Si) could be found.

Photo by Susanne Hübner, Fraunhofer Institute for Mechanics of Materials
3rd Place: black and white images
EDFAS 2011 Photo Contest

Sponsored by



ISTFA/2012

www.asminternational.org/istfa



The Materials
Information Society

Everything
Material.

www.asminternational.org

Copyright © 2012
by
ASM International®
All rights reserved

No part of this book may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise, without the written permission of the copyright owner.

First printing, November 2012

Great care is taken in the compilation and production of this Volume, but it should be made clear that NO WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, ARE GIVEN IN CONNECTION WITH THIS PUBLICATION. Although this information is believed to be accurate by ASM, ASM cannot guarantee that favorable results will be obtained from the use of this publication alone. This publication is intended for use by persons having technical skill, at their sole discretion and risk. Since the conditions of product or material use are outside of ASM's control, ASM assumes no liability or obligation in connection with any use of this information. No claim of any kind, whether as to products or information in this publication, and whether or not based on negligence, shall be greater in amount than the purchase price of this product or publication in respect of which damages are claimed. THE REMEDY HEREBY PROVIDED SHALL BE THE EXCLUSIVE AND SOLE REMEDY OF BUYER, AND IN NO EVENT SHALL EITHER PARTY BE LIABLE FOR SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES WHETHER OR NOT CAUSED BY OR RESULTING FROM THE NEGLIGENCE OF SUCH PARTY. As with any material, evaluation of the material under end-use conditions prior to specification is essential. Therefore, specific testing under actual conditions is recommended.

Nothing contained in this book shall be construed as a grant of any right of manufacture, sale, use, or reproduction, in connection with any method, process, apparatus, product, composition, or system, whether or not covered by letters patent, copyright, or trademark, and nothing contained in this book shall be construed as a defense against any alleged infringement of letters patent, copyright, or trademark, or as a defense against liability for such infringement.

Comments, criticisms, and suggestions are invited, and should be forwarded to ASM International.

ISBN-13:978-1-61503-979-1
ISBN-10: 1-61503-979-1
SAN: 204-7586

ASM International®
Materials Park, OH 44073-0002
www.asminternational.org

Printed in the United States of America

EDFAS 2012-2013 BOARD OF DIRECTORS



EDFAS President
Jeremy A. Walraven
Sandia National Laboratories



EDFAS Vice President
Cheryl Hartfield
Oxford Instruments

Board Members	Position	Affiliation
Mr. Jeremy A. Walraven	EDFAS President	Sandia National Laboratories
Cheryl Hartfield	EDFAS Vice President	Oxford Instruments
Mr. Matthew Thayer	Secretary	Advanced Micro Devices
Christopher L. Henderson	Finance Officer	Semitracks, Inc.
Dr. Thomas Moore	Past President	OmniProbe Inc., An Oxford Instruments Company
Randall S. Barnes	Executive Director	EDFAS
Dr. Philippe Perdu	Member at Large	CNES
Mr. David P. Vallett	Member at Large	IBM Systems and Technology
Mr. Nicholas Antoniou	Member at Large	Harvard University
Dr. Lee Knauss	Member at Large	Booz Allen Hamilton
Dr. William E. Vanderlinde	Member at Large	Laboratory for Physical Sciences
Mr. Zhiyong Wang	Member at Large	Intel
Board Committees	Position	Affiliation
Dr. Gernant E. Maurer, FASM	ASM BOT Liaison	Consultant
Mr. Michael Bruce	EDFA Chair	Consultant
Ms. Susan Li	Education Chair	Spansion
Dr. Zhiyong Wang	Events Chair	Intel Corporation
Dr. Philippe Perdu	International Growth Committee	CNES
Dr. Thomas Moore	Nominating Chair	OmniProbe Inc., An Oxford Instruments Company



ISFA/2012[®]

ORGANIZING COMMITTEE



Philippe Perdu
General Chair
CNES



Zhiyong Wang
Vice General Chair
Intel



Dan Bodoh
Technical Program Chair
Freescale Semiconductor



James J. Demarest
Tutorial Chair
IBM – Albany Nanotech



Ed Keyes
Tutorial Vice Chair
Solantro Semiconductor Inc.



Jeremy A. Walraven
Immediate Past General Chair
Sandia National Laboratories

Activities Chairs

Martin Keim
Audio Visual Chair
Mentor Graphics Corporation

Jerome Touzel
International Chair
Infineon

Becky Holdford
Panel Vice Chair
Texas Instruments, Inc.

Thomas Zanon
Short Course Chair
PDF Solutions, Inc.

Susan Li
International Committee Vice Chair
Spansion

Ted Kolasa
Local Arrangements Chair
Orbital Sciences Corporation

Sandra Delgado
Photo and Video Contest Chair
Nanolab Technologies

Sam Subramanian
User Groups Chair
Freescale Semiconductor

Efrat Moyal
Exposition Chair
Omniprobe Inc.

David Valett
Panel Chair
IBM

Nicholas Antoniou
Publicity Chair
Center for Nanoscale Systems, (CNS)
Harvard University

Felix Beaudoin
User Groups Vice Chair
IBM

ISTFA 2012 SYMPOSIUM COMMITTEE

ISTFA 2012 Technical Program Chair



Dan Bodoh
Freescale Semiconductor

3D Packages

YAN LI (CHAIR), INTEL
RUDOLF SCHLANGEN (CO-CHAIR),
DCG SYSTEMS

Alternative Energy

DAVID NILES (CHAIR), AVAGO
TECHNOLOGIES
CHRIS RICHARDSON (CO-CHAIR),
ABOUND SOLAR

Circuit Edit

DANE SCOTT (CHAIR), INTEL
MIKE DiBATTISTA (CO-CHAIR),
QUALCOMM

Counterfeit Electronics - Detection and Mitigation

BHANU SOOD (CHAIR), CALCE/UMD
GARY SHADE (CO-CHAIR), INSIGHT
ANALYTICAL LABS

Defect Characterization and Metrology

TERENCE KANE (CHAIR), IBM
PHIL KASZUBA (CO-CHAIR), IBM

Emerging Concepts

MIKE BRUCE (CHAIR), CONSULTANT
DAVE VALLETT (CO-CHAIR), IBM

Case Studies and the Failure Analysis Process

ROSE RING (CHAIR),
GLOBALFOUNDRIES MALTA
DAVID BURGESS (CO-CHAIR),
ACCELERATED ANALYSIS

Nanoprobing and Electrical Characterization

JOHN SANDERS (CHAIR), DCG
SYSTEMS
CHRISTIAN HOBERT (CO-CHAIR),
GLOBALFOUNDRIES

Packaging and Assembly Analysis

BECKY HOLDFORD (CHAIR), TEXAS
INSTRUMENTS
ROBERT CHAMPAIGN (CO-CHAIR),
RAYTHEON

Photon Based Techniques

FELIX BEAUDOIN (CHAIR), IBM
JIM COLVIN (CO-CHAIR), FA
INSTRUMENTS

Posters

MARTIN VERSEN (CHAIR),
UNIVERSITY OF APPLIED SCIENCES
ROSENHEIM
DAVID GROSJEAN (CO-CHAIR),
ANALOG DEVICES

Sample Prep and Device Deprocessing

BRYAN TRACY (CHAIR), SPANSION
ROGER ALVIS (CO-CHAIR), FEI

Test and Diagnosis

GEIR EIDE (CHAIR), MENTOR
GRAPHICS
MARK KIMBALL (CO-CHAIR), MAXIM



USER GROUPS

Nanoprobing

Moderators

Vijay Chowdhury
EAGLABS

Randal Mulder
Silicon Laboratories

Presentations

**The Wonderful World of Atomic Force Probing (AFP) with Applications Examples,
Its Limitations and Challenges**

Yuk Tsang
Freescale Semiconductor, Austin, Texas, USA

Advances in Nanoprobing

Stephan Kleindiek
Kleindiek Nanotechnik GmbH, Reutlingen, Germany

Nanoprobe Sample Preparation and Probe Tip Issues

Randal Mulder
Silicon Laboratories, Austin, Texas, USA

Sample Preparation Challenges and Techniques for FEOL Nanoprobing on Advanced Technology Nodes

Sean Zumwalt
Multiprobe Inc., Santa Barbara, CA, USA

Contactless Fault Isolation

Moderators

Ed Cole

Sandia National Labs

Frank Altmann

Fraunhofer Institute for Mechanics of Materials)

Presentations

Addressing 3D IC Challenges: Magnetic Field Imaging for Non-Destructive 3D Fault Isolation

Antonio Orozco

Neocera, Beltsville, Maryland, USA

The Benefits of Frequency Mapping

Chris Nemirow

DCG Systems, Fremont, California, USA

**A New Approach for Short Localization in Thin Dielectrics by
Electron Beam Absorbed Current Imaging**

Michél Simon-Najasek

Fraunhofer CAM, Halle, Germany

Focused Ion Beam (FIB)

Moderators

Richard Livengood

Intel

Mike DiBattista

Qualcomm

Presentations

Rapid Laser Material Removal for Cross Sectional Imaging for 3D Pkg Level Analysis

Jerry Lehman

Zeiss Microscopy, Thornwood, NY, USA

Multi Beam Plasma Xe/Ga FIB for Pkg & TSV FA

Drew Erwin

Tescan USA, Pleasanton, California, USA

Developing Functional Prototypes by “Package Edit” Using Plasma FIB Technology

Pete Carleson

FEI, Hillsboro, Oregon, USA

Next Generation Chemistry for Circuit Edit

Hideo Tanaka

DCG Systems, Fremont, California, USA

3D FIB/SEM at the 5 nm Voxel Scale for CE and Other IC Applications

Mike Phaneuf

Fibics Incorporated, Ottawa, Ontario, Canada

Sample Preparation

Moderators

Lucas Copeland

Texas Instruments

Jacob Klein

Texas Instruments

Presentations

Etch Rate Characterization of Palladium (Pd) Coated Copper (Cu) Bond Wires

Raymond Mendaros, Analog Devices General Trias (ADGT), Philippines

EXpressLO™ for Routine Backside Milling

Lucille A. Giannuzzi

L.A. Giannuzzi & Associates LLC, Fort Myers, Florida, USA

Safe Removal of WCSP/BGA Devices from Under-Fill Applications

Kristopher Staller

Texas Instruments, Tucson, Arizona, USA

Preparation of Wafer Level Packages Using Pulsed Laser Assisted Chemical Etching

Scott Silerman, and Robert Chivas

Varioscale, Inc, San Marcos, California, USA

Contents

2012 IPFA Best Paper

Laser Voltage Probing in Failure Analysis of Advanced Integrated Circuits on SOI	1
<i>V.K. Ravikumar¹, R. Wampler², M.Y. Ho¹, J. Christensen², S.L. Phoa¹</i>	
<i>1) Advanced Micro Devices Singapore Pte. Ltd., Singapore</i>	
<i>2) Advanced Micro Devices, Inc., Austin, TX, USA</i>	

Session 1: Emerging Concepts and Techniques

Closer to the Theoretical Limit: Spherical Corrections to Aplanatic Solid Immersion Imaging with Adaptive Optics	6
<i>Y. Lu, E. Ramsay, C.R. Stockbridge, A. Yurt, F.H. Köklü, T.G. Bifano, M.S. Ünlü, and B.B. Goldberg, Boston University, Boston MA, USA</i>	

Fault Isolation of Open Defects Using Space Domain Reflectometry	11
<i>Mayue Xie¹, Zhiguo Qian¹, Mario Pacheco¹, Zhiyong Wang¹, Rajen Dias¹, and Vladimir Talanov²,</i>	
<i>1) Intel Corporation, Chandler, AZ, USA</i>	
<i>2) Neocera, LLC, Beltsville, MD, USA</i>	

Localization of Dead Open in a Solder Bump by Space Domain Reflectometry	17
<i>David P. Vallett¹, Daniel A. Bader¹, Vladimir V. Talanov², Jan Gaudestad², Nicolas Gagliolo², and Antonio Orozco²</i>	
<i>1) IBM Technology Group, Essex Junction, VT, USA</i>	
<i>2) Neocera, LLC, Beltsville, MD, USA</i>	

Advanced Fault Isolation Technique Using Electro-Optical Terahertz Pulse Reflectometry (EOTPR) for 2D and 2.5D Flip-Chip Package	21
<i>Lihong Cao¹, Manasa Venkata¹, Meng Yeow Tay², Wen Qiu², J. Alton³, P. Taday³, and M. Igarashi³,</i>	
<i>1) Advanced Micro Devices, Austin, TX, USA</i>	
<i>2) Advanced Micro Devices (Singapore), Singapore</i>	
<i>3) TeraView Limited, Cambridge, United Kingdom</i>	

Novel Plasma FIB/SEM for High Speed Failure Analysis and Real Time Imaging of Large Volume Removal	26
<i>T. Hrnčíř¹, F. Lopour¹, M. Zdražil¹, A. Delobbe², O. Salord², and P. Sudraud²</i>	
<i>1) TESCAN a.s., Brno, Czech Republic</i>	
<i>2) Orsay Physics S.A., Fuveau, France</i>	

FemtoFarad/TeraOhm Endpoint Detection for Microsurgery of Integrated Circuit Devices	30
<i>Jim Colvin, Newark, CA, USA</i>	

Session 2: Fault Isolation and Failure Analysis of TSV

Cross Section Analysis of Cu Filled TSVs Based on High Throughput Plasma- FIB Milling	39
<i>Frank Altmann¹, Jens Beyersdorfer¹, Jan Schischka¹, Michael Krause¹, German Franz², and Laurens Kwakman²</i>	
1) <i>Fraunhofer Institute for Mechanics of Materials, Halle, Germany</i>	
2) <i>FEI Europe B.V., Eindhoven, The Netherlands</i>	
Microstructural Considerations on the Reliability of 3D Packaging	44
<i>Zhiheng Huang, Zhiyong Wu, Hua Xiong, and Yucheng Ma, Sun Yat-sen University, Guangzhou, China</i>	
High-Frequency TSV Failure Detection Method with Z Parameter	50
<i>Joohee Kim¹, Daniel H. Jung¹, Jonghyun Cho¹, Jun So Pak¹, Joungho Kim¹, Jong Min Yook², and Jun Chul Kim²</i>	
1) <i>Korea Advanced Institute of Science and Technology, Deajeon, Republic of Korea</i>	
2) <i>Korea Electronic Technology Institute, Gyeonggi-do, Republic of Korea</i>	
Enhanced Failure Analysis on Open TSV Interconnects	55
<i>F. Altmann¹, C. Schmidt¹, J. Beyersdorfer¹, M. Simon-Najasek¹, C. Große¹, F. Schrank², and J. Kraft²</i>	
1) <i>Fraunhofer-Institute for Mechanics of Materials, Halle, Germany</i>	
2) <i>ams AG, Unterpremstaetten, Austria</i>	

Session 3: Nanoprobing Techniques

A New Technique for Non-Invasive Short-Localisation in Thin Dielectric Layers by Electron Beam Absorbed Current (EBAC) Imaging	61
<i>Michél Simon-Najasek, Jörg Jatzkowski, Christian Große, and Frank Altmann, Fraunhofer Institute for Mechanics of Materials, Halle, Germany</i>	
Precise Localization of 28 nm via Chain Resistive Defect Using EBAC and Nanoprobing	67
<i>P. Larré¹, H. Tupin¹, C. Charles¹, R.H. Newton², and A. Reverdy³</i>	
1) <i>STMicroelectronics, Crolles, France</i>	
2) <i>DCG Systems Richardson, TX, USA</i>	
3) <i>Sector Technology, Gières, France</i>	
In FAB 300 mm Wafer Level Atomic Force Probe Characterization	71
<i>Terence Kane, IBM Systems Technology Group, Hopewell Junction, NY, USA</i>	
Nanoelectronic Analog Circuit PFA – The Return of Circuit Level Probing	77
<i>D.E. Albert, L. Fischer, and S. Beck, IBM, Hopewell Junction, NY, USA</i>	

Session 4: Fault Isolation and Failure Analysis of 3D Packages

Enhanced Comparison of Lock-In Thermography and Magnetic Microscopy for 3D Defect Localization of System in Packages88

Christian Schmidt¹, Frank Altmann¹, and David P. Vallett²

1) Fraunhofer-Institute for Mechanics of Materials, Halle, Germany

2) IBM Systems & Technology Group, Essex Junction, VT, USA

Non Destructive Failure Analysis of 3D Electronic Packages Using Both Electro Optical Terahertz Pulse Reflectometry and 3D X-Ray Computed Tomography95

Yan Li, Yongming Cai, Mario Pacheco, Rajen C. Dias, and Deepak Goyal,

Intel Corporation, Chandler, AZ, USA

Failure Analysis Using Scanning Acoustic Microscopy for Diagnostics of Electronic Devices and 3D System Integration Technologies100

Peter Czurratis¹, Peter Hoffrogge¹, Sebastian Brand², Frank Altmann², and

Matthias Petzold²

1) PVA Tepla Analytical Systems GmbH, Westhausen, Germany

2) Faunhofer Institute for Mechanics of Materials, Halle (Saale), Germany

Session 5: Nanoprobng Applications

Analysis of an Anomalous Transistor Exhibiting Dual-Vt Characteristics and Its Cause in a 90 nm Node CMOS Technology106

Yuk L. Tsang, Xiang D. Wang, Reyhan Ricklefs, and Jason Goertz,

Freescale Semiconductor Inc., Austin, TX, USA

Study of Static Noise Margin, Cell Stability and Influence of Electron Beam on Sub-30 nm SRAM Using SEM-Based Nanoprobng with 8 Nanoprobes112

T.H. Ng, M.K. Dawood, P.K. Tan, H. Tan, C.K. Oh, J.C. Lam, and Z.H. Mai,

GlobalFoundries Singapore Pte. Ltd., Singapore

Leaky Device Channel Anomaly Identification and Case Study by Nano-Probng Technique, Curve Fitting, and Model Analysis118

Wei-Chih Wang, Ching-Shan Sung, Ya-Hsiu Lin, Haw-Shan Chen, and Jian-Shing Luo,

Inotera Memories, Inc., Taoyuan, Taiwan, Republic of China

Session 6: Photon Based Techniques: An Understanding

Photon Emission Spectra of FETs as Obtained by InGaAs Detector123

Arkadiusz Glowacki¹, Christian Boit¹, Yoshiyuki Yokoyama², and Philippe Perdu³

1) Berlin University of Technology, Berlin, Germany

2) Hamamatsu Photonics Germany, Herrsching, Germany

3) French Space Agency, Toulouse, France

Near-Infrared Photon Emission Spectroscopy Trends in Scaled SOI Technologies	128
<i>Ulrike Kindereit¹, Alan J. Weger¹, Franco Stellari¹, Peilin Song¹, Hervé Deslandes², Ted Lundquist², and Prasad Sabbineni²</i>	
<i>1) IBM T.J. Watson Research Center, Yorktown Heights, NY, USA</i>	
<i>2) DCG Systems, Fremont, CA, USA</i>	

Characterization and TCAD Simulation of 90 nm Technology PMOS Transistor under Continuous Photoelectric Laser Stimulation for Failure Analysis Improvement	135
<i>R. Llido¹, A. Sarafianos¹, O. Gagliano¹, V. Serradeil¹, V. Goubier¹, M. Lisart¹, G. Haller¹, V. Pouget², D. Lewis², J.M. Dutertre³, and A. Tria³</i>	
<i>1) STMicroelectronics, Rousset, France</i>	
<i>2) University of Bordeaux, Talence, France</i>	
<i>3) Centre de Microélectronique de Provence, Gardanne, France</i>	

Building the Electrical Model of the Photoelectric Laser Stimulation of an NMOS Transistor in 90 nm Technology	143
<i>A. Sarafianos¹, R. Llido¹, O. Gagliano¹, V. Serradeil¹, M. Lisart¹, V. Goubier¹, J.M. Dutertre², A. Tria², V. Pouget³, and D. Lewis³</i>	
<i>1) STMicroelectronics, Rousset, France</i>	
<i>2) Centre de Microélectronique de Provence - Georges Charpak, Gardanne, France</i>	
<i>3) Université de Bordeaux, Talence, France</i>	

Session 7: Rethinking the FA Process

Words for the “Whys”	151
<i>Richard J. Ross, Essex Junction, VT, USA</i>	
EOS (Electrical Overstress) – The Old, Unknown Phenomenon?	156
<i>Peter Jacob, EMPA Duebendorf, Switzerland</i>	
DRAM Cell Fault Localization Using Passive Voltage Contrast	164
<i>San Lin Liew, Yu Pei Wei, Bi Jen Chen, Hua Sheng Chen, and Jian Shing Luo, Inotera Memories Inc., Taoyuan, Taiwan, Republic of China</i>	
3D Tomography Analysis of Dark Voltage Contrast Failure in PCRAM Device	170
<i>Jangwon Oh, Jonghyeop Kim, Taekwon Lee, Seungjoon Jeon, Won Kim, Hojung Kim, and Changreol Kim, SK Hynix Semiconductor Inc., Kyounggi-do, Korea</i>	

Session 8: Photon Based Techniques: One Step Beyond

Dual-Phase Interferometric Confocal Imaging for Electrical Signal Modulation Mapping in ICs	172
<i>A. Yurt, E. Ramsay, F.H. Köklü, C.R. Stockbridge, Y. Lu, M.S. Ünlü, and B.B. Goldberg, Boston University, Boston, MA, USA</i>	

Laser Voltage Imaging: New Perspective Using Second Harmonic Detection on Submicron Technology	176
<i>Guillaume Celi¹, Sylvain Dudit¹, Thierry Parrassin¹, Michel Vallet¹, Philippe Perdu², Antoine Reverdy³, and Dean Lewis⁴</i>	
<i>1) STMicroelectronics, Crolles, France</i>	
<i>2) CNES Laboratory, Toulouse, France</i>	
<i>3) SECTOR Technologies, Gières, France</i>	
<i>4) Université Bordeaux, Talence, France</i>	
Improving the DLS Workflow	183
<i>Dan Bodoh and Kent Erington, Freescale Semiconductor, Austin, TX, USA</i>	
Differential Polarization Imaging and Probing [DPIP]: Seeing and Probing the “Invisible”	190
<i>Baohua Niu, Martin von Haartman, Patrick Pardy, and Mitch Sacks, Intel Corporation, Hillsboro, OR, USA</i>	

Session 9: Technology Specific Case Studies

Advanced Physical Analysis Methodology for Yield and Reliability of 28-nm, Bulk-Si, Flip-Chip ICs Using SEM and Backside Deprocessing	197
<i>Yuanjing (Jane) Li, Steven Scott, and Howard Lee Marks, NVIDIA Corporation, Santa Clara, CA, USA</i>	
A Comprehensive Failure Analysis Method and Mechanism Study on Ultra-Low-K Film Adhesion Failure	203
<i>Shuting Chen, Lei Zhu, Han Wei Teo, Binghai Liu, Yanhua Huang, Kenny Ong, Zhiqiang Mo, Younan Hua, Zhaoxin Yuan, Yong Seng Heng, and Chao Yong Li, GlobalFoundries Singapore Pte. Ltd. Singapore</i>	
Systematic Approach for the Gate Oxide Failure Caused by Arsenic Cross Contamination	207
<i>Lei Zhu, Huipeng Ng, Yanhua Huang, Hanwei Teo, Kenny Ong, Shuting Chen, Changqing Chen, Ghimboon Ang, Younan Hua, and Zheng Li, GlobalFoundries Singapore Pte. Ltd. Singapore</i>	
Failure Analysis on Integrated Power Devices	211
<i>Arthur Chiang, David Le, and Huixian Wu, Vishay Siliconix, Santa Clara, CA, USA</i>	

Session 10: Photon Based Techniques: More Applications

Lock-in Phase Mapping of Modulated Reflectance in Dynamically Operating Mixed-Signal IC Devices	217
<i>Zhongling Qian, Christof Brillert, and Christian Burmer, Infineon Technologies AG, Munich, Germany</i>	

Advanced Laser Probe Techniques Applied to FA of RF Integrated Circuits - A Case Study	223
<i>Mark Kimball¹ and Christopher Nemirow²</i>	
1) Maxim Integrated Products, Inc.	
2) DCG Systems	

Case Study: Combined Dynamic Laser Stimulation and Static Emission Microscopy Techniques Applied to Scan Test Failure on Mixed Mode Device	228
<i>Magdalena Sienkiewicz and Philippe Rousseille,</i>	
<i>Freescale Semiconductor, Toulouse, France</i>	

From EBT to LVP, from 130 nm to 28 nm Node, Internal Timing Characterization Evolution	232
<i>Thierry Parrassin¹, Philippe Larre¹, Sylvain Dudit¹, Michel Vallet¹, and Antoine Reverdy²</i>	
1) STMicroelectronics, Crolles, France	
2) SECTOR Technologies, Gières, France	

Session 11: Alternative Energy

Lithium-Ion Battery Degradation Mechanisms and Failure Analysis Methodology	239
<i>Bhanu Sood¹, Lucas Severn¹, Michael Osterman¹, Michael Pecht¹,</i>	
<i>Anton Bougaev², and David McElfresh²</i>	
1) University of Maryland, College Park, MD, USA	
2) Oracle Corporation, San Diego, CA, USA	

Lock-In Thermography-Based Local Efficiency Analysis of Solar Cells	250
<i>Otwin Breitenstein, Max Planck Institute of Microstructure Physics, Halle, Germany</i>	

Challenges for Parametric Analysis of the Solar Cells Using Failure Analysis Technique Developed for the Microelectronics	255
<i>M. Boostandoost, X. Ycaza, R. Leihkauf, U. Kerst, and C. Boit,</i>	
<i>Berlin University of Technology, Berlin, Germany</i>	

Session 12: Improving Fault Isolation with Software

Filtering and Emission Area Identification in the Time Resolved Imaging Data	264
<i>S. Chef¹, S. Jacquir¹, S. Binczak¹, K. Sanchez², and P. Perdu²</i>	
1) University of Burgundy, Dijon, France	
2) CNES, French Space Agency, Toulouse, France	

Advanced Methods and Software for Enhancing Analytical Tools Capabilities during Chip Diagnostic and Characterization	273
<i>Franco Stellari and Peilin Song,</i>	
<i>IBM T.J. Watson Research Center, Yorktown Heights, NY, USA</i>	

Improved Parasitic Fault Modeling for Automatic Analog Fault Simulation	281
<i>Gerhard Borgmann, Christian Burmer, and Sébastien Mézière, Infineon Technologies AG, Munich, Germany</i>	

Time Resolved Imaging Solving FPGA Logic Fault Localization by Pattern Matching Technique	286
<i>G. Bascoul¹, P. Perdu¹, and J. Di Battista²</i>	
<i>1) Centre National d'Etudes Spatiales, Toulouse, France</i>	
<i>2) Thales Communication and Security, Toulouse, France</i>	

Session 13: Defect Analysis

SIMS Analysis for the Threshold Voltage Shift of Power MOS Caused by Abnormal Dopant Diffusion	290
<i>Yanhua Huang¹, Lei Zhu¹, Kenny Ong¹, Hanwei Teo¹, Shuting Chen¹, Younan Hua¹, Miao Shen¹, and Hao Gong²</i>	
<i>1) GlobalFoundries Singapore Pte. Ltd., Singapore</i>	
<i>2) National University of Singapore, Singapore</i>	

Study of Si Crystal Defects by Chemical Preferential Etching and Its Application on Si Dislocation Defects Caused by Laser Spike Annealing (LSA)	293
<i>Shuting Chen, Lihong Li, Anyan Du, and Younan Hua, GlobalFoundries Singapore Pte. Ltd., Singapore</i>	

A Novel Integrated Reliability Test System for BEOL TDDDB Study	297
<i>Jifeng Chen, Peilin Song, Thomas M. Shaw, Franco Stellari, Lynne Gignac, Chris Breslin, Dirk Pfeiffer, and Griselda Bonila, IBM T.J. Watson Research Center, Yorktown Heights, NY, USA</i>	

Session 14: Packaging and Assembly Analysis

Fluorosilicate Glass (FSG) Outgassing Induced Aluminum Bond Pad Corrosion during Post-Fab Wafer Storage	305
<i>Younan Hua, Ramesh Rao Nistala, and Shuting Chen, GlobalFoundries Singapore Pte. Ltd., Singapore</i>	

An Overview of Cu Wire Intermetallic Compound Formation and a Corrosion Failure Mechanism	310
<i>Dongmei Meng, Laura Buck, and James Cargo, LSI Corporation, Fort Collins, CO, USA</i>	

Lock-in Thermography for Flip-Chip Package Failure Analysis	316
<i>Lihong Cao¹, Manasa Venkata¹, Jeffery Huynh¹, Joseph Tan², Meng-Yeow Tay², Wen Qiu², Kannu Wadhwa³, and Rudolf Schlanger³</i>	
<i>1) Advanced Micro Devices, Austin, TX, USA</i>	
<i>2) Advanced Micro Devices, Singapore</i>	
<i>3) DCG Systems, Fremont, CA, USA</i>	

Dynamic Impact Package Characterization	325
<i>Jake E. Klein and Ronald R. Madsen, Texas Instruments, Tucson, AZ, USA</i>	
Development of Advanced Non Destructive Techniques for Failure Analysis of PCBs and PCBAs	332
<i>Julien Perraud¹, Shaïma Enouz-Vedrenne¹, Jean-Claude Clement¹, and Arnaud Grivon²</i>	
<i>1) Thales Research and Technology, Palaiseau, France</i>	
<i>2) Thales Global Services, Meudon La Forêt, France</i>	

Session 15: TEM Defect Detection

Four Stages of Defect Creation in Epitaxial Structures: High Resolution X-Ray Diffraction and Transmission Electron Microscopy Characterization	337
<i>Nikolai N. Faleev, Christiana B. Honsberg, and David J. Smith, Arizona State University, Tempe, AZ, USA</i>	
A Proof for the Possibility of Ce-Oxide from CMP Residuals in Si-Wafers by Analytical TEM	347
<i>Wayne Zhao¹, Liem Do Thanh¹, Michael Gribelyuk², Mary-Ann Zaitz², and Wing Lai²</i>	
<i>1) GlobalFoundries Inc., Hopewell Junction, NY, USA</i>	
<i>2) IBM at Hopewell Junction, East Fishkill, NY, USA</i>	
Tomographic Study of Silicon Nanoparticles in Nanocrystalline Non-Volatile Flash Memory Devices by EFTEM	356
<i>YongKai Zhou, Jie Zhu, AnYan Du, YouNan Hua, ZhiQiang Mo, and SiPing Zhao, GlobalFoundries Singapore Pte. Ltd., Singapore</i>	
Energy-Filtered Imaging of Polysilicon Defects, Gate Dielectric and Silicon Nanocrystals Using Plasmon Energy-Loss Electrons	359
<i>Swaminathan Subramanian, Khiem Ly and Tony Chrastecky, Freescale Semiconductor Inc., Austin, TX, USA</i>	

Session 16: Case Studies I

Analysis of Fractures of Printed Circuit Board Traces	365
<i>Carl Nail and Larry Rice, EAG, Irvine, CA, USA</i>	
Failure Analysis Methodology on Systematic Defect in N+ poly/NWELL Varactor in RF Analog_PLL due to Implanter Charging Issue	370
<i>Ghim Boon Ang, Changqing Chen, Hui Peng Ng, Soh Ping Neo, G. Magdeliza, Jony Indahwan, and Mern Tat Lee, GlobalFoundries Singapore Pte. Ltd., Singapore</i>	
Study on ATPG Failure with Butterfly Pattern	375
<i>C.Q. Chen, G.B. Ang, S.P. Zhao, S.P. Neo, A. Quah, Angela Teo, and B.H. Liu, GlobalFoundries Singapore Pte. Ltd., Singapore</i>	

Session 17: Device Level Sample Prep

- Metallic Nanoneedles Arrays for TEM Sample Preparation “Lift-Out”379**
*Romaneh Jalilian¹, David Mudd¹, Neil Torrez¹, Jose Rivera¹,
Mehdi M. Yazdanpanah¹, and Brian Miller²*
1) *NaugaNeedles, Louisville, KY, USA*
2) *Nanolab Technologies, Inc., Vancouver, W, USA*
- Deprocessing Methodologies for Detection of IBC and
Cell-to-Cell Shorts in Submicron DRAM 383**
Ramachandra Chitakudige¹, Sarat Kumar Dash², and A.M. Khan³
1) *C.M.T.I., Bangalore, India*
2) *ISRO Satellite Centre, Vimanapuram Bangalore, India*
3) *Mangalore University Konaje, Karnataka, India*
- Routine Backside FIB Milling With EXpressLO™388**
Lucille A. Giannuzzi, L.A. Giannuzzi & Associates LLC, Fort Myers, FL, USA
- High-Throughput, Site-Specific Sample Prep of Ultra-Thin TEM Lamella for
Process Metrology and Failure Analysis391**
*Roger Alvis, Jeff Blackwood, Sang-Hoon Lee, and Matthew Bray,
FEI Company, Hillsboro, OR, USA*
- Failure Analysis of Electronic Material Using Cryogenic FIB-SEM399**
Nicholas Antoniou¹, Adam Graham¹, Cheryl Hartfield², and Gonzalo Amador²
1) *Harvard University, Cambridge, MA, USA*
2) *Oxford Instruments, Dallas, TX, USA*

Session 18: Case Studies II

- Fault Isolation Techniques and Studies on Low Resistance Gross Short Failures406**
*P.K. Tan, Z.H. Mai, W.Y. Lee, Y.Z. Ma, R. He, T.H. Ng, M.K. Dawood, G.R. Low,
H. Tan, C.K. Oh, and J. Lam, GlobalFoundries Singapore Pte. Ltd., Singapore*
- A Silicon Debugging Methodology on Customer Prototype for Wafer Foundries411**
*Zhihong Mai, Tsu Hau Ng, M. Khalid Dawood, Pik Kee Tan, and Jeffrey Lam,
GlobalFoundries Singapore Pte. Ltd., Singapore*
- Failure Analysis of Nickel Silicide Piping Failures: A Case Study417**
*Clifford Howard, Yuk Tsang, Sam Subramanian, Khiem Ly, Tony Chrastecky,
Kent Erington, and Juan Ybarra, Freescale Semiconductor, Inc., Austin, TX, USA*

Session 19: Counterfeit Electronics Detection and Mitigation

- Post Decapsulation Internal Visual Inspection422**
Erik Jordan, Nisene Technology Group, Watsonville, CA, USA

Counterfeit Detection Strategies: When to Do It / How to Do It426
Greg Caswell, DfR Solutions, College Park, MD, USA

Counterfeit IC's Overview – From a Test Lab's Perspective433
Dave Looney, Premier Semiconductor Services, LLC, Tempe, AZ, USA

Session 20: Circuit Edit: Beam Interaction Studies

Characterization of Ion Beam Current Distribution Influences on Nanomachining436
*Shida Tan, Richard H. Livengood, Yuval Greenzweig, Yariv Drezner,
Roy Hallstein, and Chris Scheffler, Intel Corporation, Santa Clara, CA, USA*

Focused Ion Beam Circuit Edit on Copper Redistribution Layer440
Lorenzo Motta¹, Paolo Veneto¹, Mark Antolik², and Donato Di Donato³
1) STMicroelectronics Validation Laboratory, Agrate, Italy
2) DCG Systems, Inc., Fremont, CA, USA
3) Sector Technologies, Gieres, France

Dielectric and Metal Depositions Using Xe+ Focused Ion Beams447
Chad Rue and Brianna Carrigan, FEI Company, Hillsboro, OR, USA

**Fabrication and Characterization of Helium and
Neon Ion Deposited Platinum Wires for Circuit Edit Applications455**
*William Thompson¹, Lewis Stern¹, Huimeng Wu¹, Dave Ferranti¹, Deying Xia¹,
Fouzia Khanom¹, Philip D. Rack², Carlos Gonzales², and Michael W. Phaneuf³*
1) Carl Zeiss NTS, Peabody, MA, USA
2) University of Tennessee, Knoxville, TN, USA
3) Fibics Inc., Ottawa, ON, Canada

Session 21: Chip Level Sample Prep

Alternative Lapping Method to Reduce Edge Rounding Effect462
Hock Guan Ong and Chee Lip Gan, Nanyang Technological University, Singapore

**Simple and Fast Backside Sample Preparation Technique for
Backside Fault Localization Analysis by Using Chemical Etching Method465**
Hoon Yen Gwee and Kiong Kay Ng, Infineon Technologies, Melaka, Malaysia

Sample Preparation Challenges In WLCSP Epoxy Underfill Coating Removal471
Jason H. Lagar and Rudolf A. Sia, Analog Devices Inc., Cavite, Philippines

**Stress Reduction during Silicon Thinning Using Thermal Relaxation and
3D Curvature Correction Techniques478**
Jim Colvin¹, Heenal Patel², and Timothy Hazeldine²
1) Consultant
2) Ultra Tec Manufacturing, Santa Ana, CA, USA

Non-Chemical Solder Bump Removal Technique for Repackaging Flip Chip ICs	485
<i>Mauri Sutton, George Geoghegan, Kenneth Schopen, Kathleen Kingma, Steve Castro, Kyle Wesley, Jack Yahl, and Frank Soto, Medtronic, Tempe, AZ, USA</i>	

Session 22: Circuit Edit: Processing Strategies

Preparation of Wafer Level Packaged Integrated Circuits Using Pulsed Laser Assisted Chemical Etching	491
<i>Robert Chivas¹, Niru Dandekar¹, Scott Silverman¹, Roddy Cruz², and Michael DiBattista²</i>	
1) <i>Varioscale Incorporated, San Marcos, CA</i>	
2) <i>Qualcomm Incorporated, San Diego, CA, USA</i>	

Multi-Site Full Thickness Backside Focused Ion Beam (FIB) Editing for eDRAM Array Address Descramble Verification	498
<i>Steven B. Herschbein, Carmelo F. Scudato, George K. Worth, and Edward S. Hermann, IBM Systems & Technology, Hopewell Junction, NY, USA</i>	

VIS-NIR LED Illumination in Backside Circuit Edit and Optical Probing Applications	505
<i>Shida Tan, Richard H. Livengood, Dane Scott, Roy Hallstein, Pat Pardy, and John Giacobbe, Intel Corporation, Santa Clara, CA, USA</i>	

Session 23: Test and Diagnosis

Fault Localization Improvement through an Intra-Cell Diagnosis Approach	509
<i>Zhenzhou Sun^{1,2}, Alberto Bosio¹, Luigi Dilillo¹, Patrick Girard¹, Aida Todri¹, Arnaud Virazel¹, and Etienne Auvray²</i>	
1) <i>University of Montpellier, France</i>	
2) <i>STMicroelectronics, Grenoble, France</i>	

Logic Yield Learning Vehicle Failure Analysis in Technology Development	520
<i>Zhigang Song¹, Felix Beaudoin¹, Stephen Lucarini¹, Stephen Wu¹, Yunyu Wang¹, Lior Arie², and Kobi Steiner²</i>	
1) <i>IBM Systems and Technology, Hopewell Junction, NY, USA</i>	
2) <i>IBM Systems and Technology, Ramat Hahayal, Israel</i>	

A Novel Scan-Based Yield Enhancement Methodology for Faster Yield Ramp	526
<i>S.H. Goh¹, H.C. Lee¹, T.Y. Lim¹, Fei Ting¹, Y.T. Ngow¹, J.H. Ng¹, F.L. Kong¹, W.Y. Lau¹, S.K. Lim¹, Jeffrey Lam¹, Pan Yan², and Y.J. Liu²</i>	
1) <i>GlobalFoundries, Singapore</i>	
2) <i>GlobalFoundries, Malta</i>	

Delay Fault Model Evaluation Using Tester Response Data	532
<i>Cheng Xue and R.D. (Shawn) Blanton, Carnegie Mellon University, Pittsburgh, PA, USA</i>	

Session 24: Poster and Dessert Reception

Thermal Performance and Fabrication Improvements of Glass Interposer in 3D Packaging Systems	538
<i>M. Faqir¹, M. Bouya¹, Y. Bouissa¹, A. Elamrani¹, Z. Sbiaa¹, S.Gandhi², K.Demir², V. Sundaram², and R. Tummala²</i>	
<i>1) International University of Rabat-UIR, Sala al Jadida, Morocco</i>	
<i>2) Georgia Institute of Technology, Atlanta GA, USA</i>	
TEM/FIB Technical Solutions to Electron Beam Induced Radiation Damage to Low K/Ultra Low K Dielectrics in Semiconductor Failure Analysis	542
<i>Binghai Liu, Ye Chen, Zhiqiang Mo, Si Ping Zhao, Chue Yui Wang, and Jili Wang, GlobalFoundries Singapore Pte. Ltd., Singapore</i>	
Photon Emission Microscope as a Tool for 3-Dimensional Semiconductor Device Failure Analysis	548
<i>Steven J. Chun, Boeing Space and Intelligence Systems, Los Angeles, CA, USA</i>	
Image Reconstruction Techniques for High Numerical Aperture Integrated Circuit Imaging	551
<i>T. Berkin Cilingiroglu, F. Hakan Koklu, Euan Ramsay, Yang Lu, Abdulkadir Yurt, W. Clem Karl, Janusz Konrad, Bennett B. Goldberg, and M. Selim Unlu, Boston University, Boston, MA, USA</i>	
Two Step Fabrication of Tungsten Nanotips by AC Electrochemical Etching and Laser Irradiation for Nanoprobing on Advanced Technology Nodes	557
<i>M.K. Dawood, T.H. Ng, H. Tan, P.K. Tan, C.K. Oh, J. Lam and Z.H. Mai, GlobalFoundries Singapore Pte. Ltd., Singapore</i>	
Metallographic Investigation on Solder Creep Phenomenon	562
<i>Paul Angelo D. Gustilo and Joyce Lyn G. Fernandez, Analog Devices Inc., Philippines</i>	
A Practical Method for Trace Exposure and Roughness Measurements and Implementation in High Speed Package Design	568
<i>Valentina Korchnoy and Jacov Brener, Intel Israel, Haifa, Israel</i>	
TEM Failure Analysis and Root Cause Understanding of Nitride Spacer Bridging in 45 nm Semiconductor Manufacturing Processes	574
<i>Binghai Liu, Zhiqiang Mo, Si Ping Zhao, Yuan Yao, Kim Hong Teo, Ye Chen, Irene Tee, Gek Li Lee, Changqing Chen, Ghim Boon Ang, YOGASPARI, and Robin Tan, GlobalFoundries Singapore Pte. Ltd., Singapore</i>	
Novel Failure Analysis Sample Preparation Techniques for PoP Packaging	578
<i>Sea Chooi Ng¹, Theam Hock Chor¹, Choo Thye Ma¹, Poh Tshin Khoo¹, and Dan Bockelman²</i>	
<i>1) Intel Technology Sdn. Bhd, Malaysia, Penang, Malaysia</i>	
<i>2) Intel Corporation, Austin, TX, USA</i>	
Image and Information Enhancement by Combining Brightfield and Darkfield Optical Images	583
<i>Sonny Benson P. Rosales, Andrew C. Badillo, and Wilma R. Oblefias, Laboratory Integrated Micro-Electronics, Inc., Laguna Philippines</i>	

Scan Chain Bridge Defect on a 28 nm Technology Node Circuit, Localization Using Dynamic Power Supplies	587
<i>Thierry Parrassin, Emmanuel Petit, Guillaume Celi, Yann Mousseau, and Sylvain Dudit, STMicroelectronics, Crolles, France</i>	
Thermal Investigations on CMOS Integrated Micro-Hot-Plates Using IR Thermography	592
<i>Christian Schmidt¹, Frank Altmann¹, Giorgio C. Mutinati², Elise Brunet², Stephan Steinhauer², Anton Koeck², Martin Siegele³, Christoph Gamauf³, Alexander Nemecek³, J. Teva⁴, J. Kraft⁴, J. Siegert⁴, F. Schrank⁴, and Hans Kruschke⁵</i>	
<i>1) Fraunhofer-Institute for Mechanics of Materials, Halle, Germany</i>	
<i>2) AIT Austrian Institute of Technology GmbH Vienna, Austria</i>	
<i>3) University of Applied Sciences, Neustadt, Austria</i>	
<i>4) ams AG, Premstaetten, Austria</i>	
<i>5) InfraTec GmbH, Dresden, Germany</i>	
Low Temperature Fault Isolation Using Soft Defect Localization	596
<i>Kristopher D. Staller, Texas Instruments, Tucson, AZ, USA</i>	
Application of Scanning Probe Microscopy Techniques with Electrical Modules in Via Related Defects	601
<i>Xiang-Dong Wang, N. David Theodore, Gil Garteiz, and Paul Sanders, Freescale Semiconductor Inc., Chandler, AZ, USA</i>	
Studies of Buried Voids Capturing with e-Beam Inspection System and Confirmation with Physical Failure Analysis	606
<i>Hong Xiao and Ximan Jiang, KLA-Tencor Corp, Milpitas, CA, USA</i>	
Author Index	617